

1 CLAIMS:

2 1. A method of forming circuitry comprising:

3 forming a capacitor electrode over one region of a substrate:

4 forming a capacitor dielectric layer proximate the electrode;

5 providing a conductive diffusion barrier layer between the electrode
6 and the capacitor dielectric layer;

7 forming a conductive plug over another region of the substrate, the
8 conductive plug comprising a same material as the conductive diffusion
9 barrier layer; and

10 at least a portion of the conductive plug being formed
11 simultaneously with the conductive diffusion barrier layer.

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13 2. The method of claim 1 wherein the conductive diffusion
14 barrier layer comprises a metal nitride.

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16 3. The method of claim 1 wherein the electrode is a storage
17 node of the capacitor.

1 4. The method of claim 1 wherein the conductive plug is
2 formed within an opening in an insulative layer and wherein the
3 capacitor electrode is at least a portion of a capacitor cell plate, the
4 method further comprising:

5 before forming the capacitor electrode, forming a storage node of
6 the capacitor and forming the capacitor dielectric layer over the storage
7 node;

8 forming a protective layer over the capacitor dielectric layer before
9 forming the opening in the insulative layer;

10 protecting the capacitor dielectric layer with the protective layer
11 while forming the opening in the insulative layer; and

12 removing the protective layer before forming the conductive
13 diffusion barrier layer.

1 5. A method of forming circuitry comprising the following steps:
2 providing a substrate;
3 defining a memory array region of the substrate and a peripheral
4 region of the substrate, the peripheral region being peripheral to the
5 memory array region;
6 forming a capacitor construction over the memory array region of
7 the substrate, the capacitor construction comprising a storage node, a
8 capacitor dielectric layer, a capacitor barrier layer and a cell plate layer;
9 the capacitor dielectric layer separating the storage node from the cell
10 plate layer, the capacitor barrier layer separating the capacitor dielectric
11 layer from one of the storage node and the cell plate;
12 forming an electrical interconnect over the peripheral region and
13 in electrical connection with a doped region, the electrical interconnect
14 comprising a conductive interconnect barrier layer and a metal layer, the
15 conductive interconnect barrier layer being between the doped region and
16 the metal layer; and
17 wherein the conductive interconnect barrier layer and capacitor
18 barrier layer are formed in a same step.

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20 6. The method of claim 5 wherein the capacitor barrier layer
21 and conductive interconnect barrier layer comprise TiN.
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1 7. The method of claim 5 wherein the capacitor barrier layer
2 and conductive interconnect barrier layer comprise TiN, and wherein the
3 same step comprises chemical vapor deposition.

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5 8. The method of claim 5 wherein the capacitor barrier layer
6 and conductive interconnect barrier layer comprise TiN, and wherein the
7 metal layer comprises one or more of Ti, W, Al and Cu.

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9 9. A method of forming circuitry, comprising:
10 providing a substrate;
11 defining a memory array region of the substrate and a peripheral
12 region of the substrate, the peripheral region being peripheral to the
13 memory array region;
14 forming a capacitor construction over the memory array region of
15 the substrate, the capacitor construction comprising a storage node, a
16 capacitor dielectric layer and a cell plate layer; the capacitor dielectric
17 layer separating the storage node from the cell plate layer;
18 forming an electrical interconnect over the peripheral region, the
19 interconnect being electrically connected to the cell plate layer; and
20 at least a portion of the interconnect being formed during
21 formation of the cell plate layer.

1 10. The method of claim 9 wherein the forming the interconnect
2 and the cell plate layer comprises deposition of a common and
3 continuous conductive material over the peripheral and memory array
4 regions of the substrate.

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6 11. The method of claim 9 wherein the interconnect extends
7 between the cell plate layer and the substrate to electrically connect the
8 cell plate layer to a node elevational below the cell plate layer.

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10 12. The method of claim 9 wherein the interconnect extends
11 from the cell plate layer to the substrate to electrically connect the cell
12 plate layer to a node within the substrate.

1 13. A method of forming circuitry, comprising:
2 providing a substrate;
3 defining a memory array region of the substrate and a peripheral
4 region of the substrate, the peripheral region being peripheral to the
5 memory array region;
6 defining a first electrical node proximate the memory array region
7 of the substrate, and defining a second electrical node proximate the
8 peripheral region of the substrate;
9 forming an electrically insulative layer over the substrate and over
10 the electrical nodes;
11 forming a first opening through the electrically insulative layer;
12 forming at least a portion of a capacitor storage node within the
13 first opening and in electrical connection with the first electrical node;
14 forming a second opening through the electrically insulative layer
15 to the second electrical node;
16 in a common deposition step, forming a conductive material over
17 the storage node and within the second opening in electrical connection
18 with the second node; and
19 forming a capacitor dielectric layer and a capacitor electrode
20 operatively adjacent the storage node, one of the storage node or the
21 capacitor electrode comprising the conductive material.
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14. The method of claim 13 further comprising:

forming a first layer over the storage node layer and over the
insulative layer before etching the second opening; and
etching the second opening through the first layer.

15. The method of claim 14 wherein the first layer comprises at
least one of TiN and WN.

16. The method of claim 14 wherein the first layer comprises
TiN.

17. The method of claim 14 further comprising forming the
capacitor dielectric layer over the storage node layer before forming the
first layer.

1 18. The method of claim 14 further comprising:
2 defining a third electrical node proximate the substrate, the third
3 electrical node being proximate the peripheral region;
4 forming the electrically insulative layer over the third electrical
5 node;
6 simultaneously etching the second and third openings through the
7 first layer and through the insulative layer to the second and third
8 electrical nodes, respectively; and
9 in the common deposition step, forming the conductive material
10 within the third opening.

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12 19. The method of claim 13 wherein a portion of the conductive
13 material overlies the insulative layer proximate the second opening, the
14 method further comprising:

15 forming a protective layer over another portion of the conductive
16 material that is over the storage node layer; and

17 after forming the protective layer, removing the portion of the
18 conductive material that overlies the insulative layer proximate the second
19 opening.
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1 20. The method of claim 13 wherein the conductive material fills
2 the second opening to form a conductive plug within the second opening,
3 the method further comprising:

4 forming the capacitor dielectric layer over the storage node layer;
5 forming a metal layer over the conductive plug and over the
6 storage node layer, the capacitor dielectric layer being between the metal
7 layer and the storage node layer, the metal layer comprising at least a
8 portion of the cell electrode layer; and

9 patterning the metal layer to electrically separate a segment of the
10 metal layer comprising at least the portion of the cell electrode layer
11 from a segment overlying the conductive plug.

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13 21. The method of claim 13 wherein the conductive material fills
14 the second opening to form a conductive plug within the second opening,
15 the method further comprising:

16 forming the capacitor dielectric layer over the storage node layer;
17 and

18 forming a metal layer over the conductive plug and over the
19 storage node layer, the capacitor dielectric layer being between the metal
20 layer and the storage node layer, the metal layer comprising at least a
21 portion of the cell electrode layer and being electrically connected to the
22 second electrical node through the conductive plug.
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1 22. The method of claim 13 further comprising forming the
2 capacitor dielectric layer over the storage node layer prior to etching the
3 second opening.

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5 23. The method of claim 13 wherein the substrate comprises
6 monocrystalline silicon and the electrical nodes comprise electrically
7 conductive diffusion regions formed within the substrate.

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9 24. The method of claim 13 wherein the forming the conductive
10 material comprises forming a metal-comprising layer over the storage
11 node layer and within the second opening.

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13 25. The method of claim 13 wherein the forming the conductive
14 material comprises forming at least two layers over the storage node
15 layer and within the second opening.

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17 26. The method of claim 13 wherein the forming the conductive
18 material comprises forming at least three layers over the storage node
19 layer and within the second opening.

1 27. The method of claim 13 wherein the forming the conductive
2 material comprises:

3 forming a layer comprising TiN over the storage node layer and
4 within the second opening; and

5 forming a second layer over the layer comprising TiN, the second
6 layer not comprising TiN.

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8 28. The method of claim 13 further comprising:

9 defining a third electrical node proximate the substrate;

10 forming the electrically insulative layer over the third electrical
11 node;

12 etching a third opening through the insulative layer and to the
13 third electrical node while etching the second opening through the
14 electrically insulative layer; and

15 in the common deposition step, forming the conductive material
16 within the third opening.

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18 29. The method of claim 28 wherein the second and third nodes
19 are electrically connected through a transistor.

1 30. An integrated circuit comprising:
2 a capacitor and a conductive plug, the conductive plug and
3 capacitor comprising a first common and continuous layer.

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5 31. The integrated circuit of claim 30 wherein the first common
6 and continuous layer comprises TiN.

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8 32. The integrated circuit of claim 30 wherein the conductive
9 plug and capacitor further comprise a second common and continuous
10 layer over the first common and continuous layer.

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12 33. The integrated circuit of claim 32 wherein the first common
13 and continuous layer comprises a metal nitride and the second common
14 and continuous layer comprises a metal, the second common and
15 continuous layer being chemically different than the first common and
16 continuous layer.

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1 34. The integrated circuit of claim 30 wherein the conductive
2 plug and capacitor further comprise:

3 a second common and continuous layer over the first common and
4 continuous layer; and

5 a third common and continuous layer over the second common and
6 continuous layer.
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8 35. The integrated circuit of claim 34 wherein the first common
9 and continuous layer comprises Ti, the second common and continuous
10 layer comprises a metal nitride, and the third common and continuous
11 layer comprises one or more of W, Al and Cu; the first, second and
12 third common and continuous layers being chemically different from one
13 another.
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15 36. The integrated circuit of claim 30 further comprising:
16 a substrate;
17 an insulative layer over the substrate;
18 the conductive plug extending through the insulative layer;
19 the capacitor comprising a storage node extending through the
20 insulative layer and a cell electrode over the insulative layer; and
21 the cell electrode comprising the first common and continuous
22 layer.
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1 37. The integrated circuit of claim 36 wherein the first common
2 and continuous layer comprises TiN.
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4 38. The integrated circuit of claim 36 wherein the conductive
5 plug and the electrode layer further comprise a second common and
6 continuous layer over the first common and continuous layer.
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8 39. The integrated circuit of claim 36 wherein the conductive
9 plug and cell electrode further comprise:

10 a second common and continuous layer over the first common and
11 continuous layer; and

12 a third common and continuous layer over the second common and
13 continuous layer.
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1 40. A circuit construction comprising:
2 a substrate having a memory array region and a peripheral region
3 that is peripheral to the memory array region;
4 a capacitor construction over the memory array region of the
5 substrate, the capacitor construction comprising a storage node, a
6 capacitor dielectric layer and a cell plate layer; the capacitor dielectric
7 layer being between the storage node and the cell plate layer; and
8 an electrical interconnect over the peripheral region, the
9 interconnect being electrically connected to the cell plate layer and
10 extending between the cell plate layer and the substrate.

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12 41. The circuit construction of claim 40 wherein the electrical
13 interconnect extends from the cell plate layer to the substrate.

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15 42. The circuit construction of claim 40 further comprising a
16 transistor proximate the peripheral region of the substrate, the transistor
17 comprising a source/drain region, the electrical interconnect extending
18 from the cell plate layer to the source/drain region.

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20 43. The circuit construction of claim 40 wherein the electrical
21 interconnect and cell plate layer comprise at least one common and
22 continuous layer.
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1 44. The circuit construction of claim 40 wherein the electrical
2 interconnect and cell plate layer comprise at least two common and
3 continuous layers.

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5 45. The circuit construction of claim 40 wherein the electrical
6 interconnect and cell plate layer comprise at least three common and
7 continuous layers.